

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Cobbley et al.

Serial No.: 10/714,188

Filed: November 14, 2003

For: METHOD FOR PACKAGING FLIP-CHIP SEMICONDUCTOR ASSEMBLIES

Confirmation No.: 9360

Examiner: R. Booth

Group Art Unit: 2812

Attorney Docket No.: 2269-3437.8US
(97-0514.08/US)

Notice of Allowance Mailed:

October 14, 2005

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL995987303US

Date of Deposit with USPS: January 10, 2006

Person making Deposit: Timothy Palfreyman

TRANSMITTAL LETTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith Part B - Fee(s) Transmittal for the above-captioned application and a check in the amount of \$1715.00 in payment therefor plus five (5) copies of the patent when issued.

Also, enclosed is an Amendment Pursuant to 37 C.F.R. § 1.312(a) (13 pages), plus attached Replacement Sheets of Drawings (4 sheets) and Annotated Sheets Showing Changes

Made (4 sheets); Comments on Statement of Reasons for Allowance (2 pages); and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages).

Applicants understand that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,

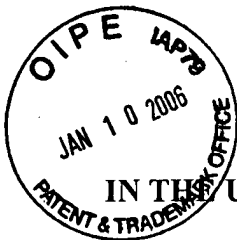


Kevin K. Johanson
Registration No. 38,506
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: January 10, 2006
KKJ/ljb:lmh

Enclosures: Part B - Issue Fee Transmittal
Check No. 22436 in the amount of \$1715.00
Copy of Transmittal Letter
Amendment Pursuant to 37 C.F.R. § 1.312(a) (13 pages), plus attached
Replacement Sheets of Drawings (4 sheets) and Annotated Sheets Showing
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Document in ProLaw



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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

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P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner indicates:

There is no prior art available nor obvious motivation to combine elements of prior art which teach a method for packaging a flip-chip semiconductor assembly, comprising: providing at least one integrated circuit (IC) die having bond pads on a surface thereof; providing a substrate having electrical pads for mounting the at least one IC die thereto; placing dry conductive epoxy dots on the electrical pads on the substrate; attaching the at least one IC die to the substrate with the bond pads of the at least one IC die in contact with the dry conductive epoxy dots on the electrical pads on the substrate to form the flip-chip semiconductor assembly with the dry conductive epoxy dots forming an electrical interface therebetween; electrically testing the flip-chip semiconductor assembly

through the electrical interface of the dry conductive epoxy dots; if the flip-chip semiconductor assembly fails testing, then reworking the flip-chip semiconductor assembly and retesting the flip-chip semiconductor assembly or scrapping the flip-chip semiconductor assembly if the flip-chip semiconductor assembly has already been reworked a preset number of times; and if the flip-chip semiconductor assembly passes testing, then encapsulating the at least one IC die on the substrate.

Applicants concur with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, the independent claims as allowed include other and different language than that specified by the Examiner, and the allowed dependent claims include other and further features and elements. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,



Kevin K. Johanson
Registration No. 38,506
Attorney for Applicants
TRASKBRITT
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